CLAIMS

1. A method for controlling the frequency of oscillation of a local clock signal comprising the steps of:

(A) generating said clock signal in response to a first control signal;

(B) generating said first control signal in response to one of a plurality of adjustment signals selected in response to a second control signal; and

(C) generating said second control signal in response to a comparison between a local timestamp and an external timestamp.

2. The method according to claim 1, wherein said second control signal is generated in further response to said clock signal.

3. The method according to claim 1, wherein said external timestamp comprises an extracted headend timestamp.

4. The method according to claim 1, wherein said extracted headend timestamp is embedded in a bitstream received from a satellite.

5. The method according to claim 4, wherein said bitstream comprises a digital bitstream.

6. The method according to claim 1, wherein said local timestamp comprises timing information in a satellite set-top box.

7. A computer readable medium configured to store instructions for executing the steps of claim 1.

8. The computer readable medium of claim 7, wherein said instructions are further configured to execute steps for controlling a satellite set tp box.

9. An apparatus comprising:

means for generating a clock signal in response to a first control signal;

means for generating said first control signal in response to one of a plurality of adjustment signals selected in response to a second control signal; and

means for generating said second control signal in response to a comparison between a local timestamp and an external timestamp.

10. An apparatus comprising:

an oscillator configured to generate a clock signal in response to a first control signal;

an adjustment circuit configured to generate said first control signal in response to one of a plurality of adjustment signals selected in response to a second control signal; and

a tuning circuit configured to generate said second control signal in response to a comparison between a local timestamp and an external timestamp.

11. The apparatus according to claim 10, wherein said plurality of adjustment signals comprise multiplexer configuration signals.

12. The apparatus according to claim 11, wherein said adjustment circuit comprises (i) a processor configured to generate

said first control signal and (ii) memory configured to store instructions for generating said first control signal.

13. The apparatus according to claim 10, wherein said external timestamp comprises an extracted headend timestamp.

14. The apparatus according to claim 10, wherein said extracted headend timestamp is embedded in a bitstream received from a satellite.

15. The apparatus according to claim 10, wherein said bitstream comprises a digital bitstream.

16. The apparatus according to claim 10, wherein said local timestamp comprises timing information in a satellite set-top box.